



# MJD44H11 (NPN), MJD45H11 (PNP)

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	71.4	$^{\circ}C/W$
Lead Temperature for Soldering	$T_L$	260	$^{\circ}C$

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^{\circ}C$ , common for NPN and PNP, minus sign, “-”, for PNP omitted, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CE(sus)}$	80	-	-	Vdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE} = 0$ )	$I_{CES}$	-	-	1.0	$\mu A$
Emitter Cutoff Current ( $V_{EB} = 5\text{ Vdc}$ )	$I_{EBO}$	-	-	1.0	$\mu A$

### ON CHARACTERISTICS

Collector-Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.4\text{ Adc}$ )	$V_{CE(sat)}$	-	-	1	Vdc
Base-Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ )	$V_{BE(sat)}$	-	-	1.5	Vdc
DC Current Gain ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 2\text{ Adc}$ ) ( $V_{CE} = 1\text{ Vdc}$ , $I_C = 4\text{ Adc}$ )	$h_{FE}$	60 40	- -	- -	-

### DYNAMIC CHARACTERISTICS

Collector Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $f_{test} = 1\text{ Mhz}$ ) MJD44H11 MJD45H11	$C_{cb}$	- -	45 130	- -	pF
Gain Bandwidth Product ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 20\text{ Mhz}$ ) MJD44H11 MJD45H11	$f_T$	- -	85 90	- -	MHz

### SWITCHING TIMES

Delay and Rise Times ( $I_C = 5\text{ Adc}$ , $I_{B1} = 0.5\text{ Adc}$ ) MJD44H11 MJD45H11	$t_d + t_r$	- -	300 135	- -	ns
Storage Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ ) MJD44H11 MJD45H11	$t_s$	- -	500 500	- -	ns
Fall Time ( $I_C = 5\text{ Adc}$ , $I_{B1} = I_{B2} = 0.5\text{ Adc}$ ) MJD44H11 MJD45H11	$t_f$	- -	140 100	- -	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MJD44H11 (NPN), MJD45H11 (PNP)

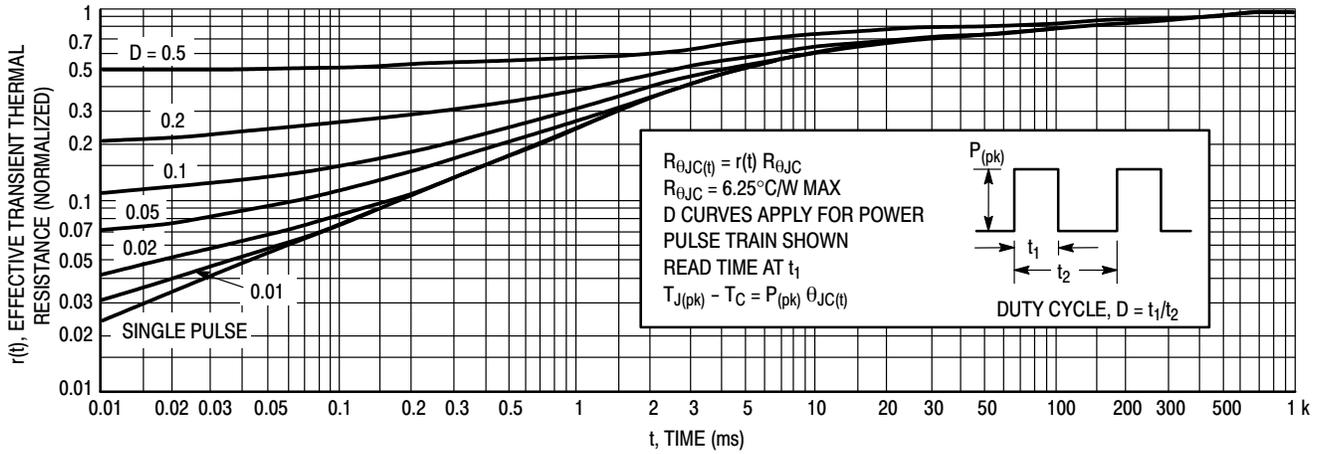


Figure 1. Thermal Response

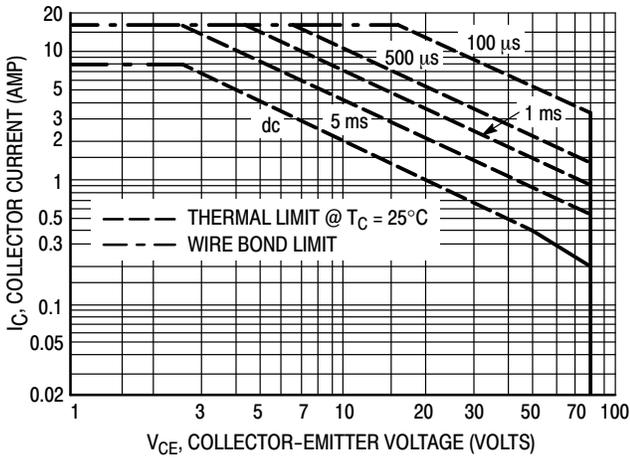


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

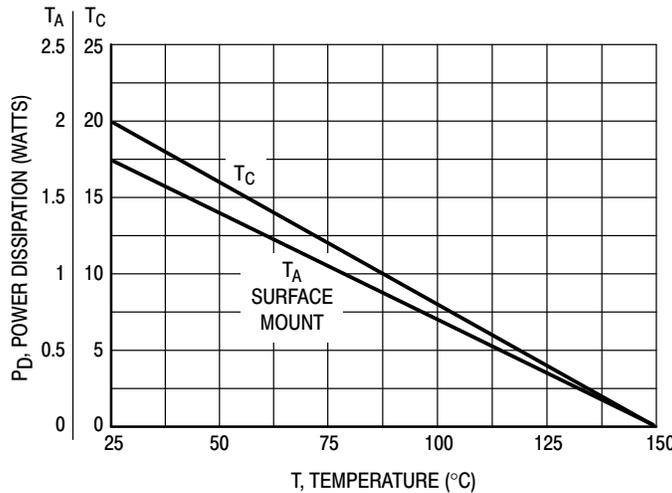


Figure 3. Power Derating

# MJD44H11 (NPN), MJD45H11 (PNP)

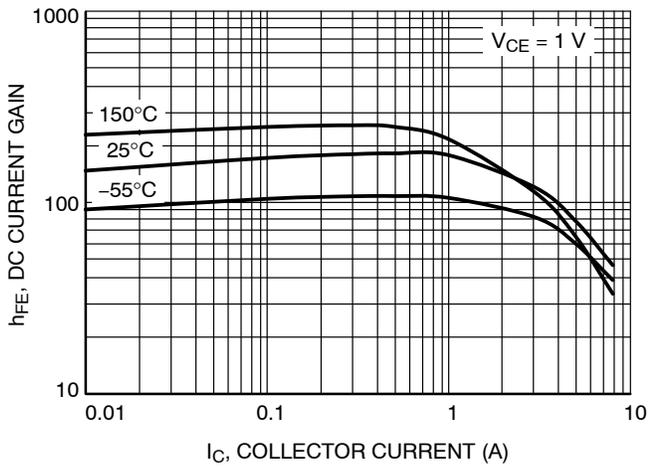


Figure 4. MJD44H11 DC Current Gain

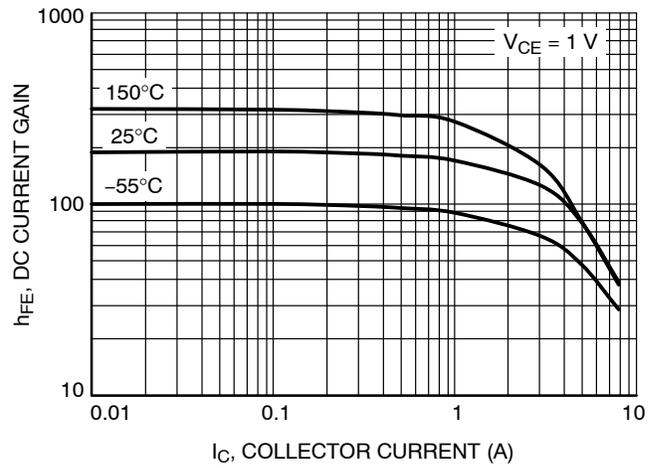


Figure 5. MJD45H11 DC Current Gain

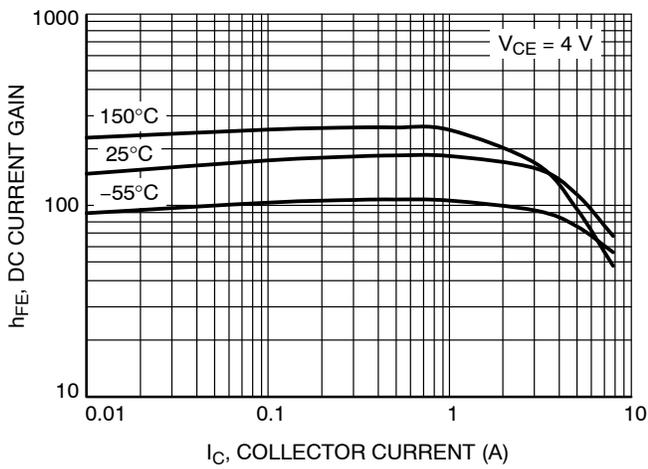


Figure 6. MJD44H11 DC Current Gain

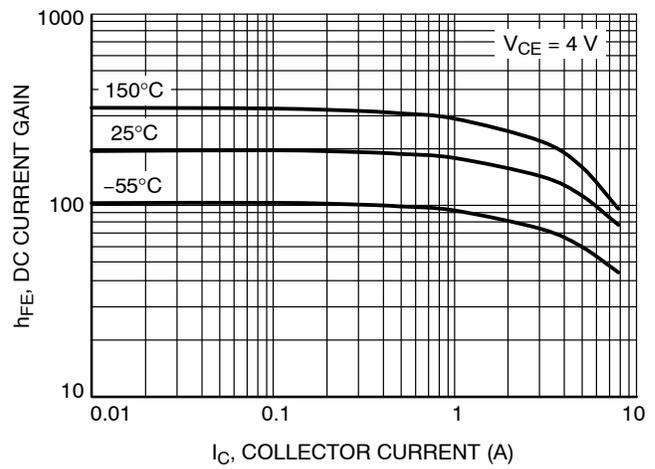


Figure 7. MJD45H11 DC Current Gain

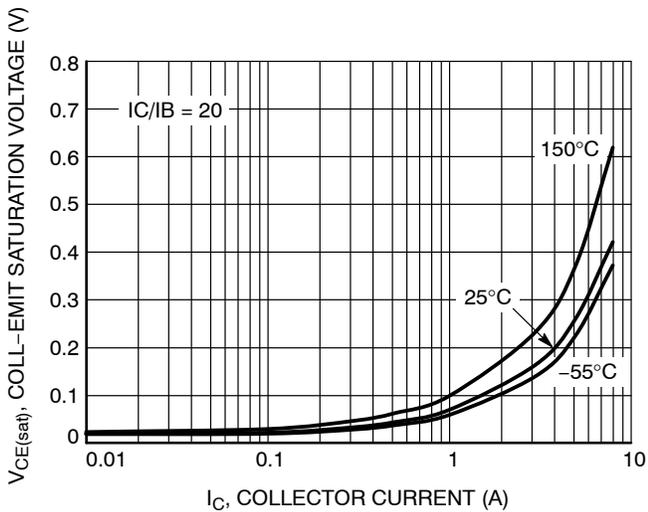


Figure 8. MJD44H11 Saturation Voltage  
 $V_{CE(sat)}$

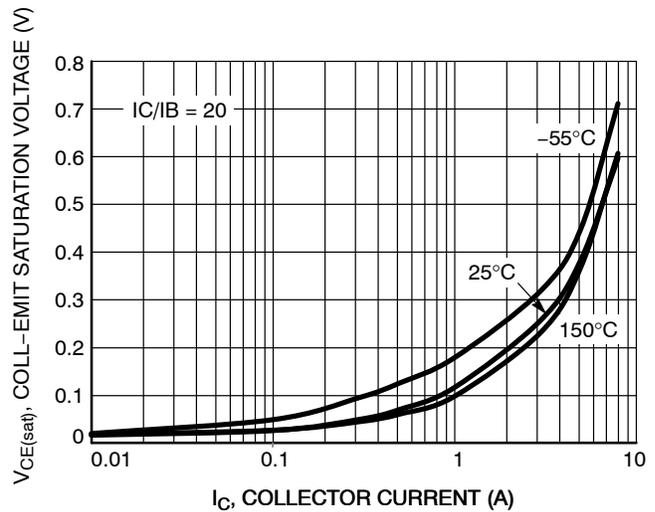
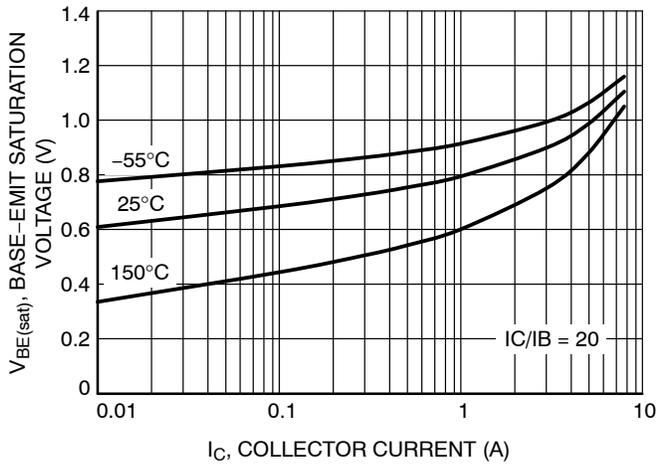
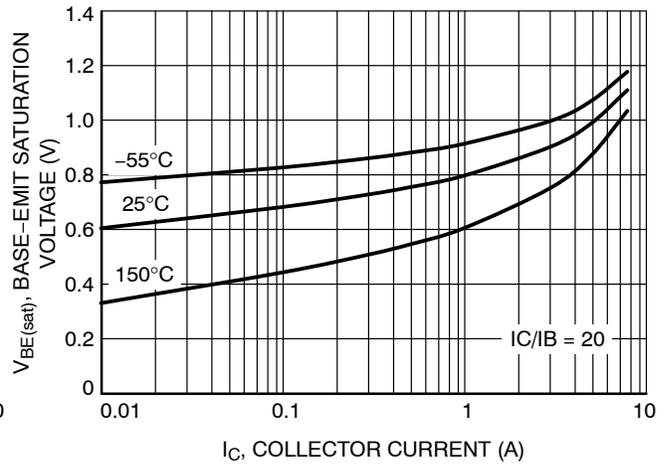


Figure 9. MJD45H11 Saturation Voltage  
 $V_{CE(sat)}$

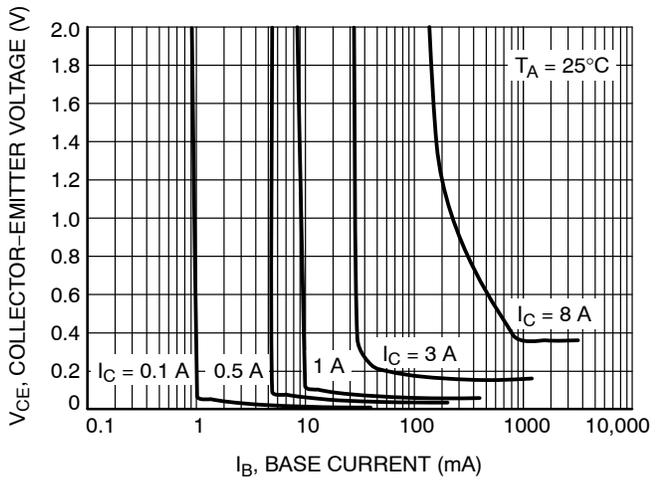
# MJD44H11 (NPN), MJD45H11 (PNP)



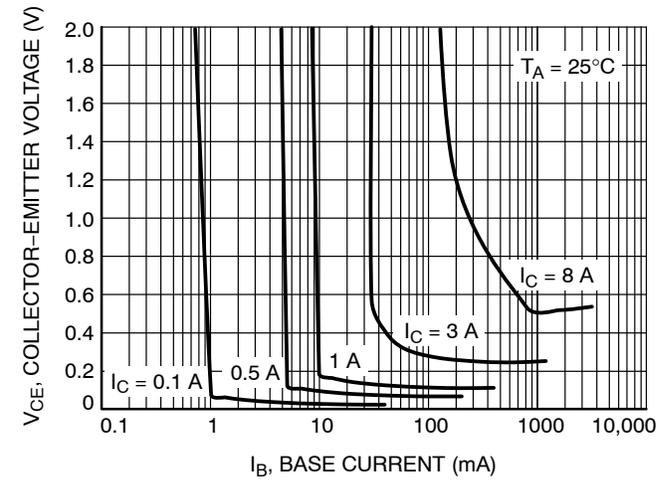
**Figure 10. MJD44H11 Saturation Voltage**  
 $V_{BE(sat)}$



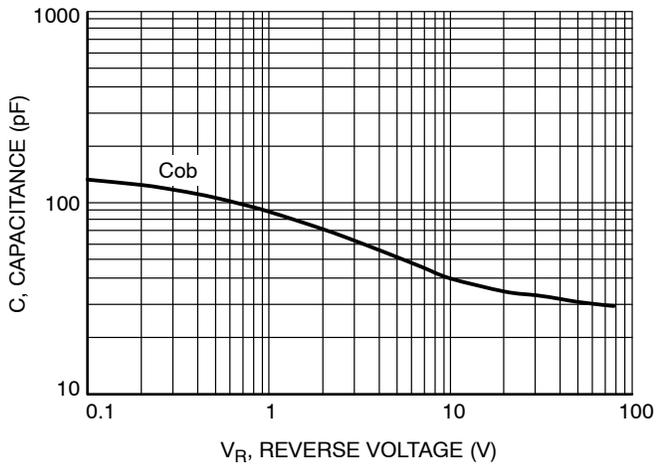
**Figure 11. MJD45H11 Saturation Voltage**  
 $V_{BE(sat)}$



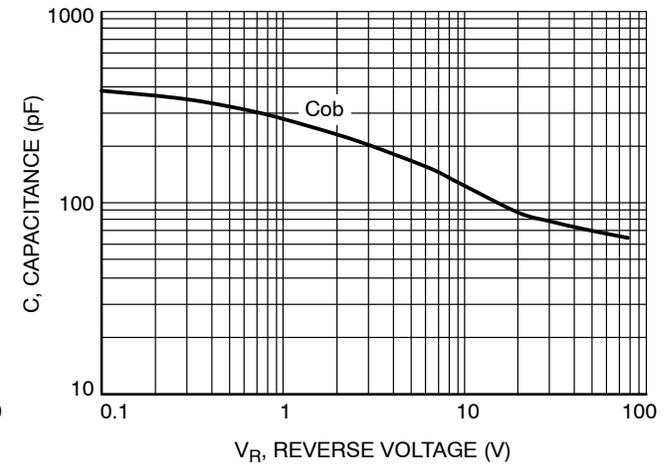
**Figure 12. MJD44H11 Collector Saturation Region**



**Figure 13. MJD45H11 Collector Saturation Region**

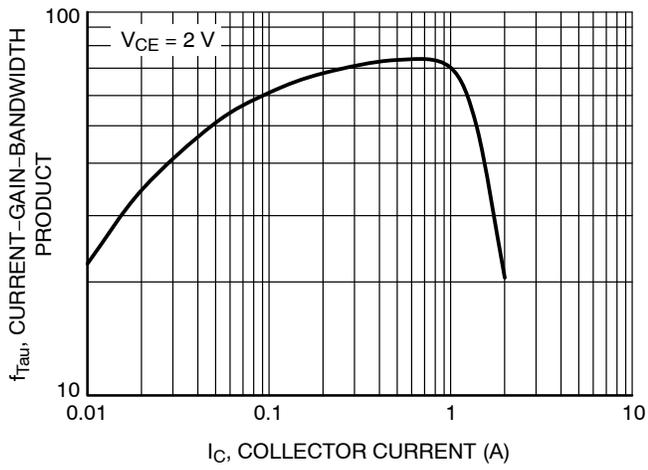


**Figure 14. MJD44H11 Capacitance**

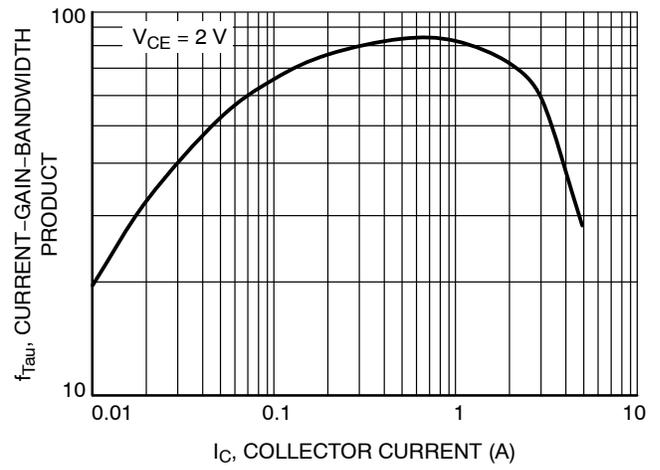


**Figure 15. MJD45H11 Capacitance**

# MJD44H11 (NPN), MJD45H11 (PNP)



**Figure 16. MJD44H11  
Current-Gain-Bandwidth Product**



**Figure 17. MJD45H11  
Current-Gain-Bandwidth Product**

## MJD44H11 (NPN), MJD45H11 (PNP)

### ORDERING INFORMATION

Device	Package Type	Package	Shipping†
MJD44H11G	DPAK (Pb-Free)	369C	75 Units / Rail
NJVMJD44H11G	DPAK (Pb-Free)	369C	75 Units / Rail
MJD44H11-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MJD44H11RLG	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
NJVMJD44H11RLG*	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
MJD44H11T4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD44H11T4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
MJD44H11T5G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
MJD45H11G	DPAK (Pb-Free)	369C	75 Units / Rail
NJVMJD45H11G*	DPAK (Pb-Free)	369C	75 Units / Rail
MJD45H11-1G	DPAK-3 (Pb-Free)	369D	75 Units / Rail
MJD45H11RLG	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
NJVMJD45H11RLG*	DPAK (Pb-Free)	369C	1,800 / Tape & Reel
MJD45H11T4G	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD45H11T4G*	DPAK (Pb-Free)	369C	2,500 / Tape & Reel
NJVMJD44H11D3T4G*	DPAK (Pb-Free)	369G	2,500 / Tape & Reel
NJVMJD45H11D3T4G*	DPAK (Pb-Free)	369G	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

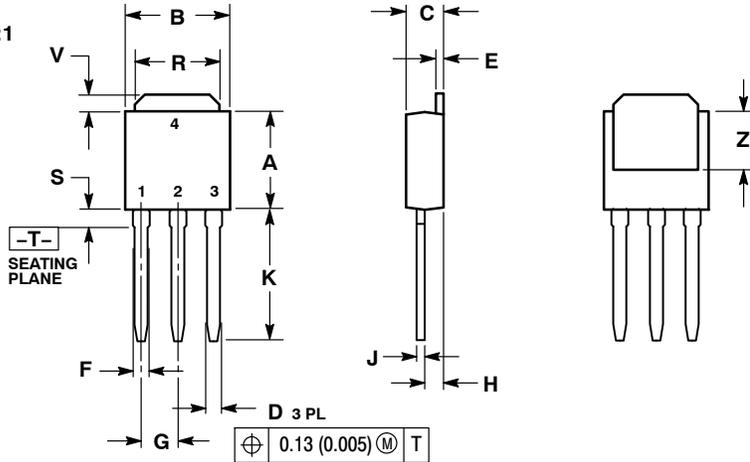
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1

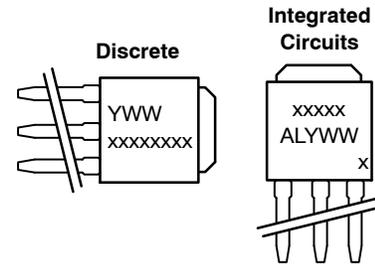


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

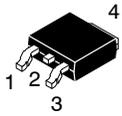
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<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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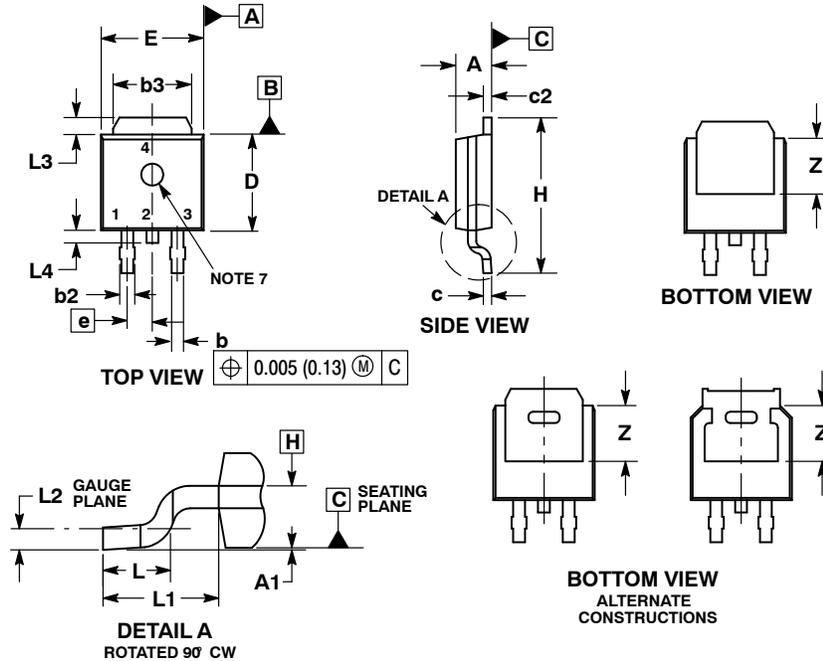
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### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

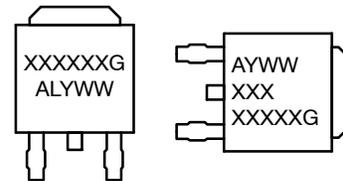


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*



IC

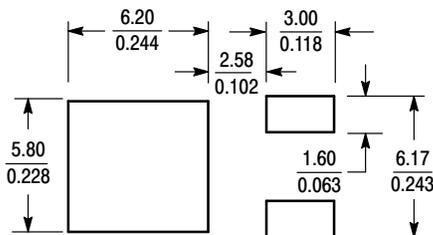
Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

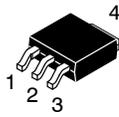
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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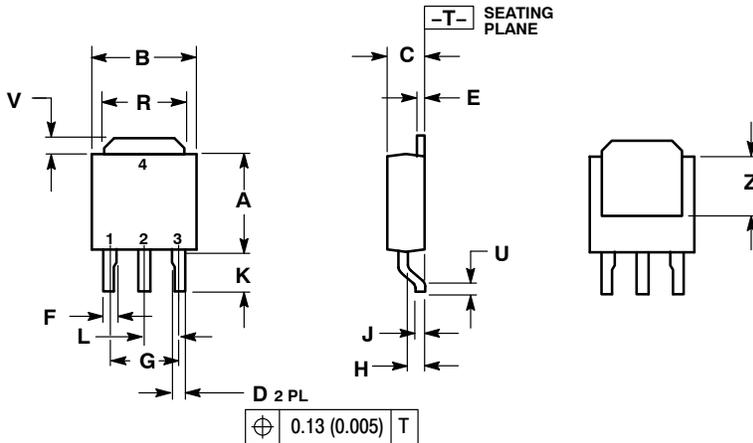
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### DPAK-3, SURFACE MOUNT

#### CASE 369G-01

#### ISSUE O

DATE 23 DEC 2003

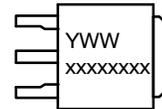


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*



xxxxxxxx = Device Code  
 Y = Year  
 WW = Work Week

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>                 PIN 1. BASE<br/>                 2. COLLECTOR<br/>                 3. EMITTER<br/>                 4. COLLECTOR</p> | <p>STYLE 2:<br/>                 PIN 1. GATE<br/>                 2. DRAIN<br/>                 3. SOURCE<br/>                 4. DRAIN</p> | <p>STYLE 3:<br/>                 PIN 1. ANODE<br/>                 2. CATHODE<br/>                 3. ANODE<br/>                 4. CATHODE</p>      | <p>STYLE 4:<br/>                 PIN 1. CATHODE<br/>                 2. ANODE<br/>                 3. GATE<br/>                 4. ANODE</p> |
| <p>STYLE 5:<br/>                 PIN 1. GATE<br/>                 2. ANODE<br/>                 3. CATHODE<br/>                 4. ANODE</p>         | <p>STYLE 6:<br/>                 PIN 1. MT1<br/>                 2. MT2<br/>                 3. GATE<br/>                 4. MT2</p>        | <p>STYLE 7:<br/>                 PIN 1. GATE<br/>                 2. COLLECTOR<br/>                 3. EMITTER<br/>                 4. COLLECTOR</p> |  |

\*This information is generic. Please refer to device data sheet for actual part marking.

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<b>DESCRIPTION:</b>	<b>DPAK-3, SURFACE MOUNT</b>	<b>PAGE 1 OF 1</b>

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